Radiation Effects Test Guideline Document for Nonvolatile Memories: Lessons Learned

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I. Introduction

The purpose of this document is to provide guidance to space flight programs and technology developers for radiation testing and qualification of nonvolatile memories (NVMs), with emphasis on modern flash memory devices. This document assumes a basic knowledge of radiation effects and of the space radiation environment on the part of the reader. It is also intended to be applicable only to the natural space radiation environment, in particular to Single-Event Effects (SEE) and to Total Ionizing Dose (TID) effects.

Nonvolatile memories (NVM) have always been an important part of spacecraft electronics. They have been used to store mission-critical data such as boot-up codes and critical flight control data, and for mass storage. Radiation and other reliability requirements vary widely, depending on the particular application. Decades ago, spacecraft NVM often meant a tape recorder. Solid state devices became more common, due to the increased reliability from not containing any moving part. This is an important advantage over many alternatives. However, solid state devices have other reliability issues, particularly when exposed to the space radiation environment. Therefore, the focus of this guideline document is to present the key results from radiation testing, identify the challenges, and discuss the lessons learned.

Nonvolatile memories onboard spacecraft systems must operate in a radiation environment consisting of electrons and ions that span the entire periodic table. Exposure to those ions may cause significant damage to critical components and compromise the mission's success. The actual particle fluxes will vary widely, depending on the spacecraft orbit, solar activity and shielding [BART97]. In some regions of space, such as in the Van Allen belts surrounding the earth, the radiation environment consists of large fluxes of electrons and protons and, and to a much lesser extent, heavy ions. Electrons cause damage primarily through spacecraft charging and TID. Protons can cause degradation through TID, SEE, and displacement damage (DD). In geosynchronous orbit or interplanetary space, galactic cosmic rays (GCR), which are predominantly ions heavier than protons, are the main component of the space environment. Solar flares and CMEs (coronal mass ejections) involve both protons and heavier ions, and can be significant in almost any orbit, although major events are relatively rare. We will discuss the impact of these radiation effects on NVM devices in this document. The process of determining the appropriate set of radiation requirement is complex [LABE98], and beyond the scope of this document. In what follows, we will focus on the radiation testing required after these levels have been determined.

II. Applicable Documents

ASTM F1192 Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices

MIL-STD-883Test Methods and Procedures for Microcircuits Method 1019 Steady State Total Ionizing Dose Irradiation Procedure

ASTM E666 Standard Method for Calculation of Absorbed Dose from Gamma or X-Radiation

ASTM E668 Standard Practice for the Application of Thermo-luminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices

USASSDC Testing Guidelines for Radiation Hardened VLSI, US Army Space and Strategic Defense Command, Huntsville, AL, Sept 1992.

NASA Proton Test Guideline Development—Lessons Learned, Aug 2002.

III. Space Environment

A full discussion of the space environment is beyond the scope of this document, but several quality reviews are available [BART97], [STASS90], [GARR93], [MAZU02], [XAPS06]. The environment encountered by a spacecraft will depend strongly on the particular orbit, and solar activity, which can vary widely over time.

In geosynchronous orbit, or in interplanetary space, GCRs are a major part of the incident spectrum, and the maximum GCR flux occurs at the minimum solar activity [TYLK97]. (It is a highly simplified explanation, but, basically, the solar wind holds back the flux of GCRs, which come from outside the solar system.) Originally, the GCR environment was represented by what came to be known as the Adams Ten Percent Worst Case Environment [ADAM84], [ADAM82]. This spectrum was based on the average GCR flux at solar minimum, but was intended to be more severe than the actual environment 90% of the time.

At lower altitudes, the radiation environment is determined largely by the trapped protons and trapped electrons in the Van Allen belts. These are best understood through a series of models, AE-1 through AE-8, and AP-1 through AP-8, where A stands for Aerospace Corp, E and P stand for electrons and protons, respectively. The model AP-8 has been incorporated into CREME96 [TYLK97]. Low energy protons [RODB07] have also been identified as a source of SEE in volatile memories, but this appears to be a very small effect, so far, in space systems. In nonvolatile memories, low energy protons have been shown to contribute only to TID damage, so far.

Depending on which orbit one selects, the maximum electron energy is in the range of 5 – 8 MeV, which is low enough that modest shielding can have a significant impact. A useful rule of thumb for electrons is that they lose about 1 MeV of energy for each 0.5 g/cm^2 of Al that they pass through. A 200 mil Al shield is about 1.4 g/cm^2. Electrons with initial energy below about 2.8 MeV are stopped completely, and those with higher initial energies penetrate the shield to the inside of the satellite, but the energy is reduced by about 2.8 MeV. Consequently, the electron fluence is significantly reduced throughout its energy spectrum. Trapped electrons are not included in CREME96, because they do not deposit enough energy to cause SEE, but they can contribute to TID effects.

The various models, AE-8, AP-8, CREME96, and others not discussed in detail here, are reasonably successful at predicting the average cosmic ray environment. However they generally do not even attempt to account for the enormous variability, which can fluctuate up to five orders of magnitude [STASS04]. With knowledge of the satellite orbit, one can predict the particle species and count (fluence), which will bombard the spacecraft over a known mission lifetime. This allows one to predict the average rate of a particular type of SEE. This knowledge can be used to guide the testing program for nonvolatile memories, or any other kind of microelectronic component. However, one cannot yet predict the environment in detail at any given time during the mission.

Detailed knowledge of the space environment is critical in determining radiation requirements, but, as a practical matter, TID and SEE are never negligible for any realistic space environment. Therefore, we will concentrate on how to perform TID and SEE testing. In the next section, we identify facilities where such testing might be done. Then we will discuss nonvolatile memory technologies to be tested, and the tests to be performed. These include heavy ion (GCR) testing, including single event latchup (SEL) testing, TID testing, and proton testing.

IV. Test Facilities

What follows is a list and brief description of some of the most commonly used testing facilities. However, there are many others, so the list is not intended to be anywhere near complete.

a. Texas A&M University Cyclotron (TAMU):
http://cyclotron.tamu.edu/ and http://cyclotron.tamu.edu/ref/index.htm
Contacts: Dr. Henry Clark and Dr. Vladimir Horvat: 979-845-1411.
Accelerator: K500 super conducting cyclotron
Energies: 8 – 70 MeV tunable and degraders in line for protons. For heavy ions, available tunes are 15 MeV/nucleon, 25 MeV/nucleon, and 40 MeV/nucleon (see Table 2). Beam intensity adjusted by accelerator operator
Beam Information: single user, beam spot is 1" diameter, 20 MHz AC beam, 50ns pulse with ns p+ pulse
Beam Location: Beam in air, in vault or in 30"D x 30"H vacuum chamber

b. Lawrence Berkeley National Laboratory (LBNL):
http://www-nsd.lbl.gov/LBL-Programs/nsd/user88/
Contacts: Dr. Rocky Koga and Dr. Peggy McMahan (510)-486-5980 p_mcmahan@lbl.gov
Or http://cyclotron.lbl.gov
Contacts: Larry Phair, lwphair@lbl.gov, or Mike Johnson, mbjohnson@lbl.gov
Accelerator: 88" K120 Cyclotron
Energies (Tune or Degraded): 1-55 MeV tuned for protons. For heavy ion, cocktails tuned to 4.5 MeV/nucleon, 10 MeV/nucleon, 16 MeV/nucleon, or 30 MeV/nucleon (see Table 3).
Beam Information: single user, up to 4" diameter beam spot collimators available, 5 – 14 MHz, 200 – 71 ns pulse with a 5 – 10 ns p+ pulse
Beam Location: vault (cave)
User Interface: Computer driven user interface with dosimetry calculation program

c. Brookhaven National Laboratories Tandem van de Graaff Facility (BNL):
http://tvdg10.phy.bnl.gov
Contacts: Chuck Carlson, ccarlson@bnl.gov, Jim Alessi, alessi@bnl.gov, Sandy Asselta, sandylee@bnl.gov, Vladimir Zajic, vzajic@bnl.gov, and Peter Thieberger, pt@bnl.gov.
Phone: 631-344-4581
Available beams: The Tandem van de Graff can deliver over 50 different ions, with Linear Energy Transfer (LET) up to 91 MeV/mg/cm^2. The Tandem van de Graaffs can now also serve as a front end, delivering ions to a Booster, which in turn delivers ions at 1 GeV/amu to the NASA Space Radiation Effects Laboratory (NSRL) [PELL10]

d. Michigan State University National Superconducting Cyclotron Facility (NSCL):
http://www.nscl.msu.edu
The NSCL is capable of delivering high Z ions at up to 200 MeV/nucleon, which means the beam has the advantage of being able to penetrate packaging materials. However, it is extremely

expensive to change ions, which means that one can usually obtain data only over a relatively narrow range of LET [LADB04].

e. Indiana University Cyclotron Facility (IUCF):
Contact Barbara von Przewoski, (812) 855-2913, or bvonprze@indiana.edu
Accelerators: Cyclotron/Synchrotron (Cyclotron only for SEE and TID) Synchrotron gives pulses of $1x10^{10}$ p+
Energies: protons up to 230 MeV peak and can be tuned or use degraders. Beam intensity adjusted by accelerator operator [JONE99]

f. University of California at Davis (UCD) Crocker Nuclear Laboratory (CNL):
Contact Dr. Spencer C. Hartman (530) 752-4218 or schartman@ucdavis.edu
The facility can provide proton beams from 1 to 68 MeV. It can also provide deuteron or alpha particle beams [CAST01]

g. NASA Goddard Space Flight Center has two ^{60}Co gamma ray sources, and two 2 MeV van de Graaff accelerators, plus a 120 keV accelerator (GSFC):
http://radhome.gsfc.nasa.gov
Contacts: Jonathan Pellish (301) 286-8046 jonathan.pellish@nasa.gov, Stephen Brown (301) 286-5975 stephen.k.brown@nasa.gov, or Kenneth LaBel (301) 286-9936 kenneth.a.label@nasa.gov
One of the ^{60}Co sources is intended for low dose rate enhanced low dose rate sensitivity (ELDRS) irradiations, and the other is intended for conventional TID testing. One of the 2 MeV van de Graaff accelerators can provide either proton or electron beams from 100 keV to 1.7 MeV. The other Van de Graaff and the 120 keV source are intended for instrument calibration.

h. Naval Research Laboratory (NRL) has two laser systems which can be used to characterize microelectronic components. The advantage of a laser system is that, because of the small spot size of the beam, it can identify small sensitive regions within the chip. One laser is a single photon system, which uses 590 nm (green) light, and which is normally used for front side exposures [MCMO06]. The second laser system uses light in the infrared (IR) spectral region (1.26 µm), which is not ionizing in Si [LADB09]. For this reason, Si is transparent to the beam, except when the light is focused to the point where charge is produced via simultaneous absorption of two photons (TPA). The TPA system is used for back-side illumination, and normally requires some thinning of the substrate.
Contacts: Stephen Buchner Stephen.buchner@nrl.navy.mil, or Dale McMorrow dale.mcmorrow@nrl.navy.mil

i. TRIUMF, Vancouver, BC, Canada http://www.triumf.ca
Accelerator: Cyclotron (for more facility information see: http://www.triumf.ca/pif/)
Energies (Tune or Degraded): 60 MeV – 500 MeV for protons on two lines with variable energy extraction 65 to 120 MeV (line one) & 180 to 500 MeV (line two); degraders to cover gap and

down to 20 MeV; two lines in the same vault, both simultaneous and completely independent with fluxes of 100 to 10^8 or 10^9 p/cm^2/s (smaller beam spot for 10^9). For electronics testing, the facility is usually used as a proton source, but it is also used heavily for nuclear physics research, and can deliver a wide variety of other beams.

j. RADEF, University of Jyvaskyla, Finland https://www.jyu.fi/fysiikka/research/accelerator

k. GANIL, Caen, France http://www.ganil-spiral2.eu

l. SIRAD, Padova, Italy, http://sirad.pd.infn.it

V. Nonvolatile Memory Technology

The dominant commercial NVM technology is floating gate (FG) flash memory. The storage element is a poly-crystalline Si element, which is surrounded by insulators, as shown in Fig. 1. Electrons are injected at high field from the substrate through the tunnel oxide into the floating gate for the Write operation (logic zero state). The process is reversed to Erase the cell to the logic one state. The electric field is reversed, and electrons are injected back into the substrate. Flash memories are available in either of two alternative architectures, which are illustrated in Fig. 2. The NAND architecture has a serial organization, where perhaps 32 bits are connected in a string, with one set of source and bit line contacts. In the NOR organization, each cell has its own contacts, which allows random access. The NAND memories are usually used for mass storage of data due to the higher density and faster Program/Read/Erase operation modes. The NOR memories are often used to store critical control codes due to its capability to access individual cells. NAND memory is by far the most popular commercial NVM option due to the demand for mass storage coupled with its relatively low cost per bit. Generally, flash memory has the advantages of low weight, low cost, and low power consumption, which are important both in handheld electronics and in space systems.

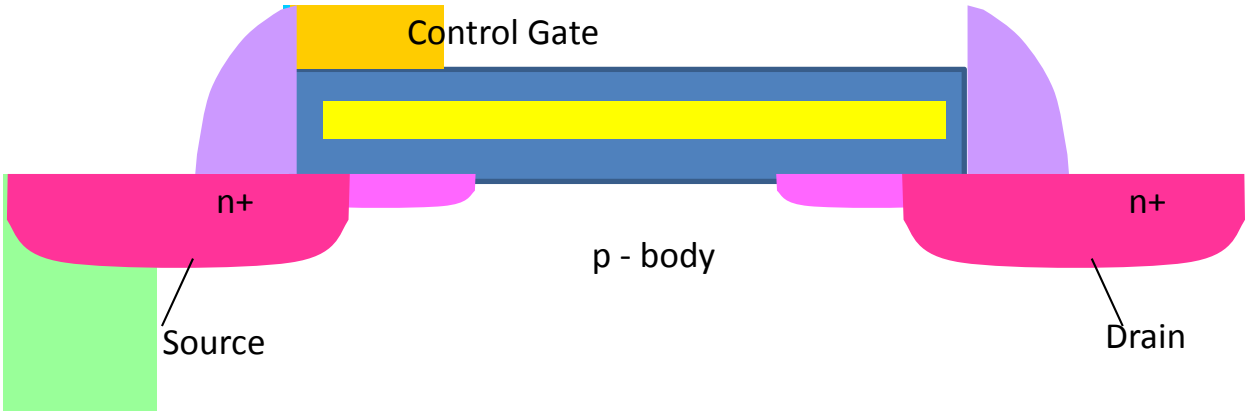

Fig. 1. Floating gate flash memory cell, with poly-Si storage element completely surrounded by insulators (blue).

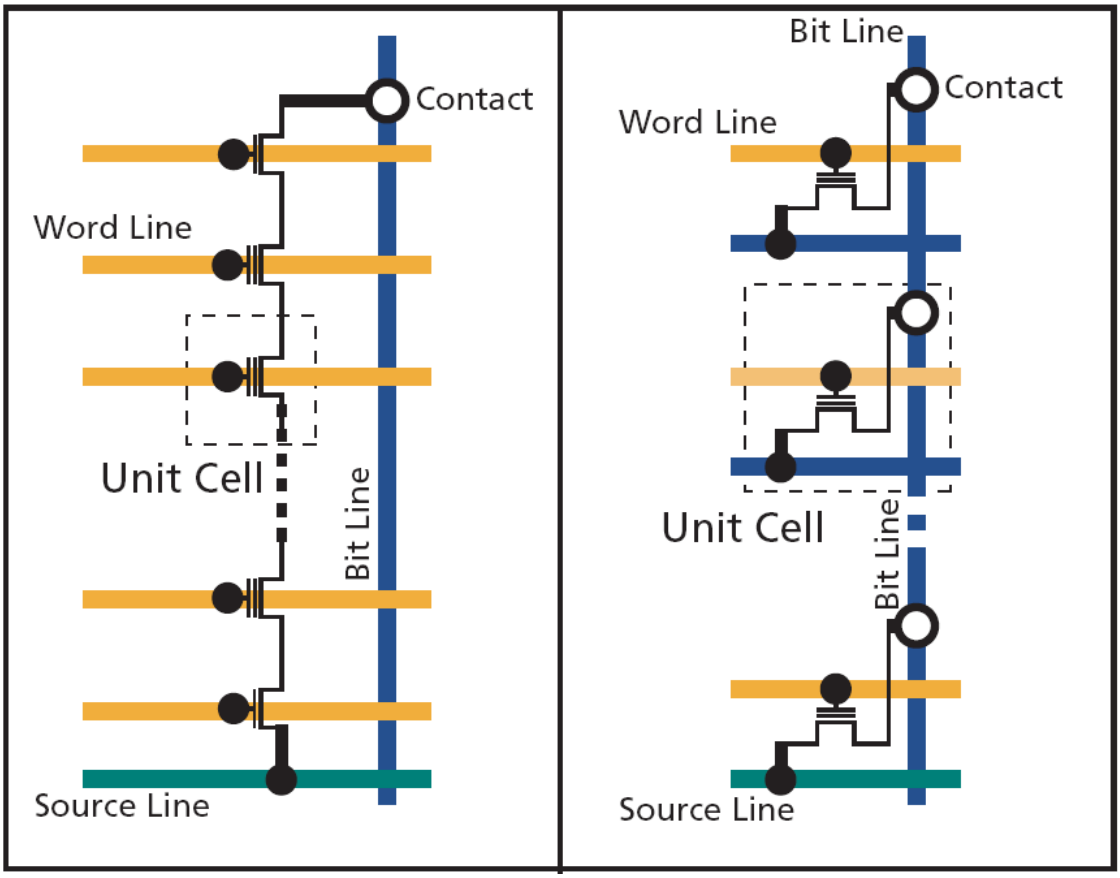

Fig. 2. (a) NAND flash memory with serial organization, and (b) NOR flash, with direct access organization.

Other types of commercially available NVM technologies include phase change memory (PCM), magneto-resistive memory (MRAM), ferroelectric memory (FERAM), organic memory (ORAM), and conductive-bridge memory (CBRAM). PCM has a chalcogenide storage element which can be switched between amorphous (high resistance) and crystalline (low resistance) phases. The most advanced PCM available is currently 128 Mb, compared to flash memories of 64 Gb, or even more. The MRAM can be polarized into high or low resistance states, but the most advanced product currently available is 4 Mb. The FERAM has a residual electric polarization, either positive or negative, which can be sensed electrically, but the largest memory currently available is 8 Mb. Organic memory stores data in an organic material with reversible resistive switching properties. Conductive bridge memory or programmable metallization cell technology consists of two layers of electrodes with a thin film of electrolyte between them. A voltage higher than the threshold is applied to the positive terminal, which results in redox reactions, driving the metal ions into the electrolytic film. The ions form a conductive bridge between the electrodes. Applying a negative voltage to the positive terminal turns off the device.

We also note that flash memory technologies that do not use floating gates are also entering production. The storage element is usually a charge trapping layer (Si_3N_4, for example) or a Si nanocrystal layer. The difference is usually transparent to the user, however. The nonvolatile storage element in the cells is relatively radiation resistant in all these technologies, but the readout and peripheral control circuits are all unhardened commercial complementary metal oxide semiconductor (CMOS) based, and all have the limitations associated with unhardened commercial CMOS.

These alternative NVM technologies have faster Read performance relative to flash memory. Some of these technologies also exhibit better Write performance. In addition, they do not require charge

pumps for Write/Erase operations (with the exception of ORAM). However, in spite of the performance advantages, these emerging technologies cannot match the storage density of flash. The market maturity of flash memory ensures its present dominant status. Furthermore only flash NVM has been flown in space, to our knowledge. Therefore, the rest of this document will concentrate on flash memory testing, although other NVM technologies will be discussed when appropriate.

VI. Lessons Learned

The appropriate test methodology should adequately evaluate the degradation characteristics for the given type of radiation. The degradation behavior varies depending on the device operation configuration and beam parameters. Due to the complexity of the commercial flash technologies, time and budget do not allow testing for every combination of operation mode and beam parameters. Therefore, one must identify the applicable operation conditions and understand the degradation and/or failure mechanisms.

a. Single-Event Effects

As with other highly scaled CMOS technologies, SEE performance of flash is an important radiation assurance concern. However, the floating gate architecture makes the flash technology intrinsically resistant to charge leakage, so the flash cell array is naturally robust against ion-induced upsets. Heavy ion testing has revealed that the control circuit, especially the charge pump, contains the most SEE sensitive components. Single particle hits on the sensitive nodes in the control circuit can result in page and/or block errors. Consequently, large amounts of data can be lost, or portions of the memory can become unusable without erasing and reprogramming. In the worst cases, strikes in sensitive nodes, such as the charge pumps, can cause destructive failures.

The selection of appropriate beam parameters is pertinent for heavy ion testing. The considerations include the ion linear energy transfer (LET), energy, range, flux, and fluence. In general, the ions should have sufficiently high energy to penetrate the sensitive volume, so that the Bragg peak LET value reflects the energy deposited within the sensitive volume. The particle flux should be kept low enough to avoid multiple ion effects. The particle fluence should be sufficiently high to draw statistical confidence, especially for low count events like single-event functional interrupt (SEFI) and single-event latchup (SEL).

Laser testing is sometimes utilized to identify, by location, sensitive regions on the die. There are currently two types of laser systems available for SEE characterization – single and two photon absorption. The latter is typically used through backside illumination, which is necessary when the topside of the die is difficult to penetrate – *e.g.* due to topside metallization.

Proton testing is sometimes necessary if the device has a relatively low LET threshold for heavy ion-induced upsets. High-energy protons are used to determine the limiting upset cross section. Testing with lower energy protons may be required to find the upset threshold energy. The appropriate test energies should simulate the range of energies that the part is expected to be exposed to in space. Protons also generate total ionizing dose with a recombination rate similar to ^{60}Co irradiation. Therefore, one must be mindful of the TID-induced degradation when irradiating to high fluence levels. Interestingly, although many flash devices have shown relatively low upset threshold from heavy ion testing, they have not exhibited SEE sensitivity to proton irradiation.

b. Displacement Damage

Current flash technologies are fabricated with CMOS processes, which are relatively less susceptible to displacement damage than bipolar processes. Although heavy ions can also cause displacement

damage, the magnitude is generally negligible given the total exposure fluences involved on the ground or in the space environment.

c. Total Ionizing Dose and Reliability

The procedures for TID testing remain fairly standard and are defined in MIL-STD-883 Test Method 1019. Flash technologies are based on CMOS processes, so enhanced-low-dose-rate-sensitivity (ELDRS) is not an issue. The bias conditions should simulate the application conditions as closely as possible. The parts will remain in static bias, standby mode, or powered off most of the time in typical applications. So dynamic mode testing, where the flash is cycled constantly during irradiation, is not necessary. The device should be written with checkerboard patterns, so that both logic 0 to 1 and logic 1 to 0 type errors can be examined. In addition, one set of parts should be cycled in between each exposure to verify the program and erase functions.

Combined TID and reliability studies should also be implemented in some cases. The combined effects more realistically simulate the device conditions in space. The test involves irradiating the flash devices to a dose less than the failure dose. Then the parts are placed in a life test for 1000 hours at elevated temperature and overstress voltage for accelerated aging. The temperature should ideally be 100 ^{o}C. However, the temperature may be reduced to the maximum specification temperature allowable for the part if that value is below 100^{o}C. The combined effects studies have shown that TID exposure can increase retention errors. However, the implementation of error correcting codes will detect and correct most of the bit errors.

The degradation characteristics from TID testing are memory array errors and control logic errors, similar to SEE testing results. The memory array errors are mostly single-bit flips, while control logic errors can result in block errors or destructive failures. So, while the number of bit errors increase with total dose, degradation to the control circuits often results in a significant increase in the error count. The radiation hardness of the control circuit largely determines the part's usability. We describe the different types of radiation effects and test methodologies in more detail and draw conclusions.

VII. Heavy Ion Testing

It is almost impossible to comprehensively test a complex advanced integrated circuit due to the various combinations of beam parameters and device operating conditions constrained by time and budget. LaBel et al. have estimated that a complete test matrix for one synchronous dynamic random access memory (SDRAM), with all its operating modes, would require about 66,000 hours of beam time [LABE08]. A leading edge NAND flash memory is almost as complicated. Therefore, one has to make trade-offs to achieve the best possible test coverage. Our goal in this section, as in the rest of this guideline document, is to provide guidance about how to make these trade-offs.

a. Beam Parameters

Ion species, energy, LET, particle range, flux, and fluence are all parameters that are typically chosen by the experimenter. Beam uniformity is another important parameter, which is usually controlled by the facility operators. These parameters are not independent, so choosing them normally involves compromises. For example, the energy of the ion species determines its LET and range. The heavier ions typically have a higher LET, but a shorter range. The ion penetration range may become an issue for complex flash memory devices, where there are several layers of metallization shielding the sensitive die. TAMU and LBNL have sufficiently high beam energies, so that ion penetration generally does not become an issue. Both TAMU and LBNL have a system with five scintillator detectors to monitor beam uniformity and flux rate (other facilities generally have something comparable). One detector is in the

center, the DUT position, and four others are around the center on the edge of the beam. When the beam conditions are adjusted so that the detectors are consistent within a few percent, the center detector is removed, and the DUT is positioned in the beam path. The remaining four detectors continue to monitor the beam, so that any changes in the beam can be detected immediately. Generally, achieving reasonable uniformity in NVM testing is not a big issue due to the small size of the die. For example, the beam at TAMU is nominally one inch in diameter, while commercially available NVM chips are typically only 1-2 cm^2 in area.

It is desirable to obtain data at several different LETs to map out the cross section curve. Typically, it is necessary to determine the saturation point, the threshold point, and a few data points in between the former points that determine the shape of the curve. A Weibull distribution is typically used as the preferred failure distribution, although other distributions can also be used for the data fits. The Weibull distribution has four parameters, so at least four points are necessary to determine a unique solution. As a practical matter, the LETs to be used determine which ions have to be used. There are trade-offs to consider at each LET. The high LET particles are generally less penetrating—the faster the particles lose energy, the sooner they come to rest. Penetration depth is important, especially in SEL (single-event latchup) testing, because the SEL mechanism involves current flows along conduction paths relatively deep in the substrate. Sufficient ion range is necessary to activate these conduction paths. There have been cases reported where SEL was observed at TAMU (with the beam energy at 15 MeV/nucleon), but not observed with the same ion on the same part, at, for example, BNL, where the relatively lower energy beams have less penetration depth. The other case where limited range may be important is in testing for angular effects. At high angles, a short range particle will penetrate even less than usual and may not always go all the way through the active device region. LBNL can deliver a standard cocktail of ions at 4.5 MeV/nucleon, but the beam is much less penetrating than the same ions at TAMU. Experimenters working with short range ions should be aware of the limitations, so that they can adjust their experimental plan, when necessary. We note that there are higher energy cocktails at LBNL that may be suitable.

The second necessary trade-off involves flux, fluence, and the optimum use of beam time. Generally, one wants to test to high fluence for sufficient coverage of the sensitive locations and for statistical confidence. On the other hand, one also wants to keep the flux low enough to avoid collective effects. In space, the flux is extremely low, so effects will always be due to single ion interactions. However, the cyclotron facilities offer flux rates as high as 10^4 to 10^5 particles/cm^2·sec. Therefore, flux effects such as double ion strikes are possible. The remaining problem is that running to high fluence at low flux is not an efficient use of beam time. A run to 10^7 particles/cm^2 at 10^4 particles/cm^2·sec requires 10^3 sec, which might be justified. At 10^3 particles/cm^2·sec, the same run would require 10^4 sec, which is much harder to justify. One strategy that might be employed is to do a few beam runs at high flux to high fluences to look for unusual destructive events, which might be extremely rare in space. Then, in separate runs, one can go at much lower fluxes, to lower fluences, to characterize the “normal” response to the typical space environment. However the experimenter chooses to approach accelerated testing, trade-offs will have to be made because beam time will always be limited. It is important for experimenters to understand what they are giving up in making these trade-offs.

b. Part preparation

For many heavy ion sources, the ion beams are not energetic enough to penetrate typical packaging materials. This includes TAMU and LBNL, which are probably the most commonly used sources, at least in the US. As we have already mentioned in the discussion of facilities, there are high energy sources, which are capable of penetrating almost any electronic package, but these facilities have other drawbacks, usually cost or convenience. Therefore, special handling will usually be necessary to prepare

the test samples for the beam, and we will discuss possible ways to do this, and common pitfalls, in the rest of this section.

The commercial nonvolatile memory with a dominant market share is floating gate NAND flash, which frequently comes in a plastic encapsulated 48-pin thin small outline package (TSOP), which is an industry standard package. This package is 1.2 cm by 2.0 cm in area, with a thickness of 1.4 mm. The most common configuration is a metal lead frame with the die on top of it where the top surface of the die faces up. To expose the top surface of the die, one has to etch the plastic off the top surface of the package. Different organizations seem to use their own recipe for this etch step, so it is best to consult with the chemistry lab that will actually do the etch step in order to decide on the etch recipe.

Nitric acid (specifically, 98% red fuming nitric acid) is typically used for chemical decapsulation. Bare, unmounted parts can be semi-automatically etched using a commercial etching solution, such as the Nisene JetEtch (Fig. 3), which sprays a vortex of heated nitric acid through a specifically-sized gasket to create the desired window in the plastic. This is often the procedure used for TSOP-style parts which will be placed in a socket on the test board and is the easiest way to repeatedly etch large numbers of parts. A certain amount of trial-and-error is usually required to find the right "recipe" for a given package. This recipe will be a specific combination of acid temperature, acid volume, etch time, etc., and will be specific to the part to be etched and equipment used. After etching, each part should be rinsed in acetone and thoroughly dried to minimize any oxidation on the metal surfaces. Fig. 4 shows parts that have been decapsulated with a jet etching process.

Fig. 3. Nisene JetEtch II automatic jet etcher.

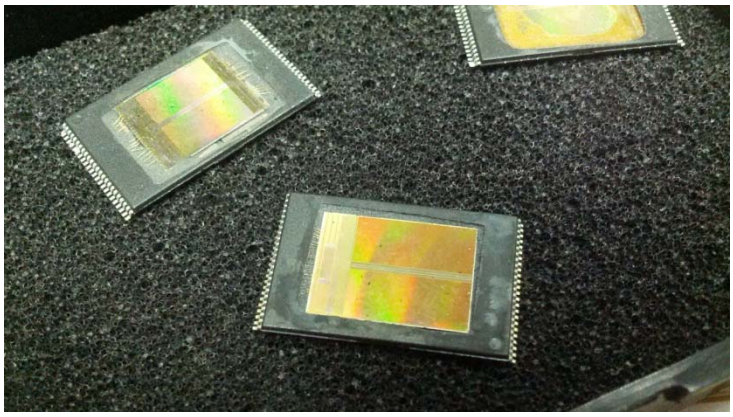

Fig. 4. Flash memories etched with nitric acid using a jet etcher.

Ball grid array (BGA) packages are also common. There is no industry standard for BGA packages. In fact, different BGA packages are sometimes used for different technology generations, even within the same company. If the die is in a flip chip configuration, face down on the substrate, one also has to thin the die to allow the beam to reach the active device region of the chip. Plastic etching of BGA packaged parts is preferably performed manually after the parts are soldered to a test board. Etching these parts prior to soldering, while easier, may not be compatible with the automatic pick-and-place equipment used for board assembly and solder reflow. Instead, the user will carefully place acid on the plastic area to be etched. A mask must be used to prevent the acid from running onto the board and damaging other components or the electrical traces. Fig. 5 shows a photograph of a delidded BGA packaged device already mounted on a board. While a general recipe may be helpful, there will be far more part-to-part variability in the hand-etching process, so the process should be carefully monitored and may require adjustment. When hand-etching with nitric acid, proper safety procedures should always be followed in an appropriate chemical lab environment.

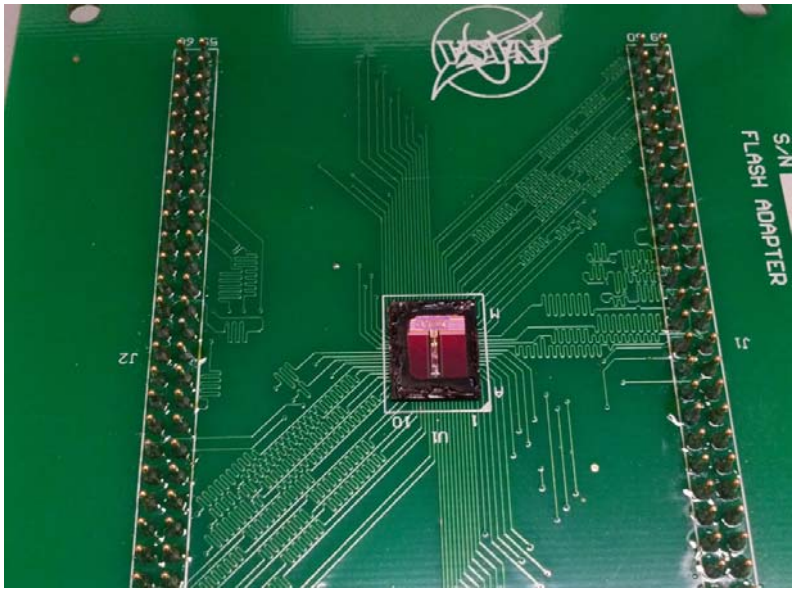

Figure 5. Flash memory which has been hand-etched after board assembly.

There are at least two complications that can arise due to the device packaging technique. First, it is possible to obtain parts which contain stacked die. For example, a 32 Gb part may really be a four-high stack of 8 Gb chips, or, for that matter, an eight-high stack of 4 Gb chips. These stacks have to fit in the same 1.4 mm thick TSOP package as a single die, so the die have to be thinned significantly before they can be stacked. This means that some beams will penetrate more than just the top die. However, it is difficult to get reliable data from anywhere except the top die. For this reason, it is very important to determine the physical to logical correlation—die number 1 is not necessarily the top die, so it is important to determine which die is on top. This can usually be done by reading out all the dice on the first shot. After that, one can save test time by concentrating on just the top die. The second complication is that etching the plastic package or etching to thin the die will sometimes damage the chip. Yield will generally not be 100%, so the experimenter should plan on some losses in deciding how many chips to prepare.

c. Sample Size

The number of devices tested is typically constrained by budget, beam time, and part availability. That said, the US Department of Defense has a Test Guideline document, which recommends at least three parts be used in any SEE test [USAS]. The radiation response can be highly variable for unhardened commercial technology, which includes state-of-the-art NVM technology. This is why one would want to have data on at least three parts for statistical confidence. One also must take into account part failures due to package decapsulation and functional failures during testing.

d. Testing at Speed

Generally, testing should be done at a frequency as close as possible to the actual application operational frequency. By now, it is well established that the rate of single-event transients (SET) and single-event upsets (SEU) is proportional to the operating frequency. The SET rate will likely be underestimated if the test frequency is less than the operational frequency. However, nonvolatile memories generally operate at much lower frequencies than high-speed logic devices, or devices with high data throughput rates. For example, leading edge flash memories currently operate at 40 MHz, whereas GHz frequencies are not uncommon in other applications. Even so, testing at speed is not without challenges. The use of FPGA-based test systems, such as the NASA Low Cost Digital Tester, have made it much easier to test at relevant application speeds [HOWA06].

e. Pattern Sensitivity

In a flash memory, a cell is empty of electrons in the logic 1 state (after an Erase operation), and full of electrons in the logic 0 state (after a Write operation). Since the effect of radiation is usually to introduce positive charge into the insulating layers, radiation exposure tends to change logic 0 into logic 1. Therefore, all zeroes is the most sensitive test pattern for single bit errors. However, control logic errors can introduce errors of both polarities. For this reason, it is common to test with a checkerboard pattern. Modern flash memories have many billions of bits, so testing a portion of the entire memory (for example half of the bits) is generally sufficient for statistical confidence. But it is at least arguable that control logic errors are the most important effect—one ion can cause millions of errors from a control logic failure. The same ion will cause only one or a few single bit errors. Generally, we check every bit in both the logic 0 and logic 1 state after a heavy ion exposure.

We note that other kinds of NVMs generally do not function by storing charge. Phase change memory depends on a resistance change in the storage element; magnetic memory depends on magnetic polarization, ferroelectric memory depends on electric polarization, and so on. Therefore, other NVMs do not have the same kind of pattern sensitivity.

f. Test modes

Nonvolatile memories have many operating modes, not all of which can be tested, for reasons explained in [LABE08]. Therefore, it is important to concentrate on the applicable operating modes. For example, some manufacturers have a cache mode for I/O operations, where an additional I/O buffer is available. For the sake of test efficiency, one may examine the response of the part with cache mode at the beginning of the run, and continue with the remainder of the test without cache mode, if there is no significant difference. Furthermore, some manufacturers may have a Read for Copy Back mode, which allows a Page to be copied to another location, without using any external I/O buffer. The purpose is to improve throughput in solid state disk (SSD) applications. These features may not be applicable to every application. Therefore one should design the test around the particular application, or the most widely used test conditions. Ordinarily, there are a few test modes that are relevant in typical floating gate flash memory applications: (1) Static mode, without bias (grounded); (2) Static mode, with bias; (3) dynamic Read mode; (4) dynamic Read/Write mode; and (5) dynamic Read/Erase/Write mode. Other kinds of NVM do not necessarily have a separate Erase operation, in which case there is no need to test it. One option that is attractive to flight programs is to power down components when they are not in use. Unpowered components are typically much less susceptible to SEE. However, we have observed a functional failure and a destructive event at relatively low LETs in an unpowered flash memory [Oldham 2006]. Nonvolatile memories are likely to be in Static mode (even when powered) during their normal operating life span, so it is important to determine the SEE characteristics for the case of biased Static mode. Static mode tests are performed by writing a pattern, irradiating, and counting errors after turning off the beam. Dynamic Read mode tests are done by reading the part continuously with the beam on, and counting the errors. This method captures both static errors and dynamic errors, which are due to transient (ion-induced) noise in the Read circuit. Normally, we do a separate Read of the entire memory, after turning off the beam. The post-irradiation Read operation determines and distinguishes the number of static bit errors and transient errors. The procedure for a Write test in flash memory includes reading a block, and rewriting any errors that are detected, during irradiation. The Write operation involves injecting electrons into a floating gate, which is empty of electrons—that is, the operation only corrects one polarity of errors (zero-to-one). The Write operation corrects both polarities of errors for most other NVMs. The test system counts the number of errors corrected, but there may not be any errors left to count at the end of the run. Flash memory has a separate Erase function, so the Erase step necessarily precedes the Write step, with a typical test order of Read/Erase/Write/Read. A block is Read and Erased if any errors are detected. Then it is rewritten, and Read again to verify that the Erase and Write operations were successful. Both the Erase and Write operations require a charge pump to put out ±10V. Single event-induced functional failures often originate from the charge pump circuits. The high voltage operations are introduced one at a time to isolate their effects.

Figure 6 shows the SEU cross section vs. LET for a 2 Gb commercial flash device, irradiated under static mode condition at NSCL and TAMU. Figure 7 shows the SEU, SEFI, and destructive event cross sections vs. LET, irradiated under dynamic Read/Write/Erase mode. Evidently, more severe SEE modes (SEFI and destructive events) appear during the dynamic test, which exercises more control circuit components, including the charge pump. Therefore, when testing modern flash devices, it is important to evaluate a comprehensive set of test conditions, including static and dynamic modes, to produce a complete picture of the SEE response.

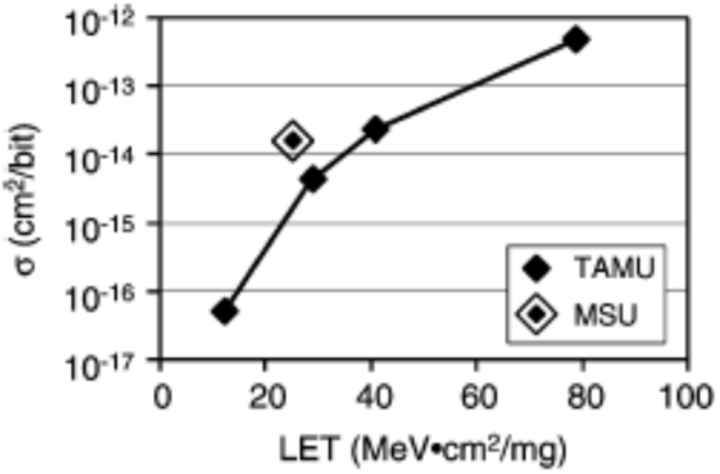

Figure 6. Static mode SEU cross section. (After[OLDH06-B]).

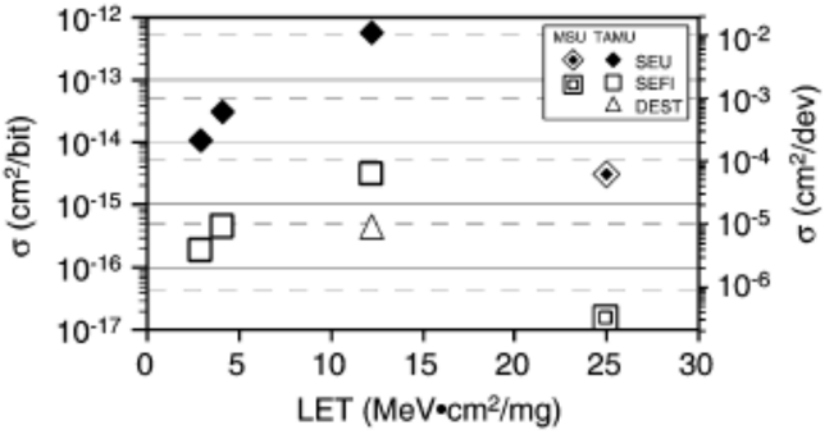

Figure 7. Dynamic Read/Write/Erase SEE cross section. (After[OLDH06-B]).

g. Angular Effects

Angular effects in standard volatile memories are known to have significant impact on the SEE response. Angular effects are relatively less critical in nonvolatile memories, such as flash, owing to the different physical mechanisms. In a volatile memory, such as a SRAM, an angular strike can leave an ion track deep into the sensitive volume. Charge collection and diffusion occurs for the entire ion track throughout the entire sensitive volume. The collected charge can "pull down" the voltage on sensitive nodes for every cell along the track, leading to simultaneous upsets of multiple cells. In a nonvolatile memory such as flash, the storage element is typically physically isolated from the substrate, so charge collection and diffusion from the substrate will have no direct effect on the floating gate. The floating gate of the flash memory is surrounded by insulators, which prevent the charges collected in the substrate from reaching the floating gate. The ion will need to hit the floating gate to cause an upset. Other kinds of NVM, such as phase change memory or magnetic memory, are similar in that the storage element is isolated from the substrate by insulating layers. Therefore, the cell arrays in a nonvolatile memory are less sensitive to angular effects than in other types of memory technologies. Nonetheless, studies have observed angular effects in some flash memories. Cellere et al. have shown that in highly

scaled circuits an ion track can hit multiple cells since the cells are smaller than the diameter of the track [CELL07]. Therefore, an incident ion can deposit charges in a cell while not necessarily passing through the floating gate of that cell.

The control logic of a nonvolatile memory is usually sensitive to high-angle ions, just as control logic would be in any other memory. The voltages on critical nodes can be changed by charge diffusing from the substrate, over a wide area, regardless of whether or not the memory is nonvolatile. Angular effects on the control logic may be more important than effects on the cell array, particularly in NVMs. We specifically discuss the radiation effects on the control logic in a later section.

h. Single-Event Functional Interrupts

This section discusses recoverable SEFIs, which are control logic errors, but not permanent failures. Flash memory, like most other advanced memories, are extremely complex chips with an on-chip controller to operate the memory for the user. The problem is that a single particle-induced controller error can result in millions or even billions of errors. Several studies have observed SEFIs in different flash memory technologies during dynamic Read, Read/Write, and Read/Erase/Write mode testing [OLDH06-B], [BAGA10].

SEFIs vary widely, and are difficult to distinguish and categorize. Statistics on SEFIs are usually poor, due to the variety of SEFI types and lower rate of occurrence. For some manufacturers, the most common SEFI is a block error, where all of the bits in a block become either all logic zeroes or logic ones. Cycling power restores normal operation, and the stored information, which was not corrupted, can be recovered. Other SEFI types can result in permanently lost data, which can only be recovered from a backup system. Critical information always has to be backed up adequately, and this is another reason why care has to be taken.

i. Destructive (Functional) Failures

Nonvolatile memories are vulnerable to destructive events or functional failures during heavy ion testing. In principle, heavy ions can trigger a SEL in almost any CMOS structure [TANZ97], [IROM01]. The only requirement is to have an NPNP or PNPN silicon controlled rectifier structure. SEL is a self-sustaining high-current condition, which can burn out metal lines if it persists long enough. The worst case test condition for latchup is at high temperature and high voltage [TANZ97]. A test device temperature of 125 °C and a test bias of nominal voltage +20% are recommended [TANZ97]. Commercial parts, which are not intended to operate at 125 °C, should be tested at the highest operating temperature indicated on the manufacturer's specification sheet, which is often 70 °C, and at nominal voltage +10% (usually 3.6 V) for current generation flash devices. In a SEL test, we start at the highest LET and work down in LET. If no latchup is observed at a given LET, there is no point in continuing testing at any lower LET. If SEL is observed, cycling power is the only way to restore normal operation. Sometimes, however, high-current conditions are observed that are not true SELs, which can be cleared with a simple DUT reset or even a command to stop Writing, for example. These other steps should always be tried first, with a power cycle following, only if necessary. When time allows, rather than simply turning off the power supply, we will gradually reduce the voltage in steps of 0.1 V to determine the holding voltage (the voltage necessary to sustain the latched condition). There is some risk in doing this, however, because the longer the high current is sustained, the more likely it is that something will burn out, destroying the part. On the other hand, we sometimes allow the current to remain high for a reasonable period, to see whether the SEL is destructive or not. Latent damage to metal lines has been observed after "non-destructive" SEL, however, which means some damage is done, even when the part is still fully functional [BECK02].

The control and peripheral circuits in Flash devices contain components that are most vulnerable to destructive events and functional failures. These circuits contain charge pump circuits [DICK76], [TANZ97], which, by definition, put out voltages higher than the input power supply voltage. For NAND flash, these voltages are typically in the range $\pm$ 10 V, compared to nominal power supply voltages of 3.3 V. To perform the Write function in a NAND flash, +10 V is typically applied to the cell control gate and -10 V is applied to the substrate, which means about 20 V total is applied across the tunnel oxide. The Erase operation is similar, except the polarity is reversed. Both operations proceed by Fowler-Nordheim (FN) injection of electrons, either into the floating gate or out of it for NAND flash. NOR flash, on the other hand, writes by Channel Hot Electron (CHE) injection, with FN Erase. When functional failures occur, it normally means that either the Erase function or the Write function stops working, or, often, both. These failures are normally attributed to the charge pump, because the only functions that have failed are those that require the charge pump. If the charge pump circuit no longer puts out enough voltage to support Fowler-Nordheim injection, processes that require FN injection would be expected to stop, which is what is normally observed. Irom et al. [IROM01] have monitored the charge pump output directly during heavy ion exposure. They found that the voltage put out by the charge pump dropped from about 20 V initially, to something less, and usually much less, when functional failure occurred. This result confirms what had been assumed without direct proof, previously. Although the duty cycle for these high-voltage operations is usually low, on the order of at most a few percent, a prudent test procedure will emphasize these operating modes, because they produce most of the functional failures, which are the most serious consequences.

Moreover, destructive current spikes have been reported [IROM01], which are said to come from the charge pump. These spikes are reportedly 300-400 ms in duration, and current levels can be 80 mA, or more. However, follow-up tests have not confirmed these reports [OLDH11]. High currents were sometimes observed, but they were usually changes in the DC current level, which persisted for tens of seconds or minutes. Similar effects have been reported in the literature for combinational logic circuits, which did not have charge pumps [SHIN05], [LABE92], [POIV04]. The correlation between functional failure and high-current events was tenuous, at best. Examples of high current without failure, and of failure without high current were presented. In addition, one example was presented where there appeared to be a failure due to SEGR (Single-Event Gate Rupture). Once the gate oxide was shorted out, of course there was high current, but it appeared to be the result of the failure, and not the cause. Laser testing will be discussed later, but a laser test found many locations in the control logic where high currents could be induced; none of them appeared to be in the charge pumps. Current spikes are still sometimes discussed, but experimenters should be aware of the more recent contrary evidence, as well as the early reports supporting them.

j. Data Analysis: Correlation of Event Rates in Space with Ground Test Results

It is important to correctly correlate ground test results with mission flight conditions, due to the significant differences in the test and space environments. One may argue that a ground test is an extreme over-test. Ground testing often involves high LET ions and high particle flux and fluence, which are several orders of magnitude higher than what the spacecraft would experience through a typical mission lifetime. The flux in geosynchronous orbit for ions at or above the LET of Au is about one particle/cm^2 every 7200 years [ADAM84]. At the LET of Xe, the flux is about one particle/cm^2 every 125 years. Furthermore, the high LET ions are preferentially eliminated by geomagnetic shielding in lower earth orbits. It will take more than 7 x 10^{10} years to accumulate 1 x 10^7 Au ions/cm^2 in geosynchronous orbit, assuming present conditions.

In many cases, one may also use heritage data as an argument for radiation assurance. While heritage data is invaluable, it is pertinent that the data are used in the correct context for evaluating event probability. For example, the Samsung 8 Gb NAND flash (K9F8G08U0M) has been tested on

multiple occasions at accelerators. Functional failures (destructive events) and destructive events have been reported [IROM07], [OLDH11]. Nevertheless, ESA (European Space Agency) has launched its PROBA-II satellite, with a TDM (Technology Demonstration Module) which contains four of the Samsung 8G die [HSOR11-A], [HSOR11-B] into an 800 km polar orbit. After more than a year in orbit, they have not observed any SEFI or destructive events. The only notable SEE events were eight single bit errors, which were corrected by the on-chip error correction software. The performance in space has been essentially flawless, despite the results obtained under extreme conditions [IROM07], [OLDH11]. However, the heritage data provide limited statistical significance. For example, we can calculate the probability of a destructive event or functional interrupt, based only on the heritage data, assuming a successful event-free 10-year mission. The upper bound for the expected number of events, with 0 event observed, is 2.3 at the 90% confidence level. Therefore, the probability of experiencing ≥ 1 event in a similar mission is 21%, with 90% confidence. Will a flight program accept the risk of flying the part purely based on the 21% probability of failure as determined from heritage data?

The Electronic Industries Association test procedures JESD-57 recommend ≥ 100 events per data point [JESD96]. However, it is practically impossible to obtain such high event counts for SEFIs and destructive events. In those cases, test standards generally require testing to a fluence of 10^7 particles/cm^2. This ensures coverage of one particle per 10 μm^2, which is adequate for the feature sizes of older technologies. However, the feature sizes have diminished to submicron dimensions with continuous scaling. Consequently, this raises the question of whether a fluence of 1×10^7 particles/cm^2 is adequate for testing modern devices with deep submicron processes. In [LADB07], Ladbury *et al*. provides an analysis on the statistics of SEE rate prediction for large and small event counts.

An important tool for estimating the rate of errors and other events in space is the code CREME96 [ADAM84], which is still widely used, despite limitations that are widely recognized. The code requires an experimental cross section curve as a function of LET. The measured curve is fitted with a Weibull curve [WEIB51], which requires determining four fitting parameters. These Weibull parameters, plus other information about the device geometry and the desired orbit, are the necessary inputs. CREME96 then calculates an error rate for the specified device in the specified orbit. One of the problems with CREME96 is that it was originally written when the cells of memory devices were much larger than the diameter of an ion track. The track was treated as line, a set of points with no width, which either intersected the device sensitive volume or not. With continued scaling, which has proceeded faster in NAND flash than in any other technology, this assumption is no longer true. The cells are now smaller than the track diameter and geometrical effects are more complicated—and more important—than previously recognized. For this reason, upgrades to CREME96 have been in progress [WELL10] for a while. Both the original CREME96, and the upgraded version called CRÈME-MC (for Monte Carlo), are available at [CREME]. It is expected that CREME96 will continue to be useful, because it was a standard for many years and because it is a way to compare new results with previously published results. Comparing results from the old code with the new code is also a good way to see how much difference the code changes really make. Eventually, though, the new code will become the standard, because it incorporates more of the real radiation transport and device physics. Another useful method for estimating error rates in space is Petersen's Figure of Merit (FOM) [PETE83], [PETE98], [NORM04] although we will not discuss it in detail here.

k. TID and Micro-Dose

Heavy ions also contribute to accumulated ionizing dose. Most heavy ion facilities have software available that will calculate the TID on each beam run, so the user can keep track of the accumulated TID. These software packages typically work by multiplying the ion LET by the total number of ions incident. However, the calculated dose values do not account for recombination effects. Columnar recombination from heavy ions will typically reduce the effective dose by 90 to 99% from the stated

values, depending on the ion and the applied field [OLDH81], [OLDH85]. Even without the recombination correction, it usually takes many runs at high LETs to approach the TID failure level for a typical NVM. The advanced NVM devices, such as flash memory, are generally impervious to the dose levels typically seen in heavy ion tests, as we further discuss in the TID section. Therefore, accumulated dose from heavy ions is typically not a concern. However, heavy ions can cause micro-dose effects in individual transistors.

Micro-dose is total dose damage deposited by a single ion. Micro-dose effects have been shown to be significant in SRAMS [39, 40], DRAMS [SWIF94], and power MOSFETs [SHAN08], [LIU08]. However, the effect of micro-dose is less clear in flash memories. Cellere *et al*. showed that the amount of charges lost from the floating gate in a heavy ion-induced bit flip is much larger than the amount of charges deposited by the ion that escape recombination [CELL01], [CELL02]. They suggest that the trapped charge lowers the potential barrier to tunneling in a localized region, thus creating a conductive path, allowing charge from the floating gate to escape to the Si substrate [CELL01], [CELL04-A]. The tests were carried out on 350 nm technology devices; 34 nm node devices are available now. The amount of charge loss necessary to flip a bit has scaled with area, so the charge deposited by the ion, which escapes recombination, is approximately equal to the amount required to flip a bit. This does not mean that the conductive path mechanism is no longer present, but it is possible that it is no longer the dominant process. In any case, other effects have been observed, which clearly suggest that micro-dose has measurable effects. For example, apparent bit flips have been observed to anneal [SCHM07], [GUER06]. Charge trapped in the oxide causes a threshold voltage shift in the cell, without discharging the floating gate. If the V_T shift is large enough, the cell is read as discharged even though it has not really been discharged. When the oxide trapped charge anneals, the cell is then read correctly, again. In addition, stuck bits have occasionally been observed in flash memories, which would be expected if an undischarged cell that appears to be discharged cannot be reprogrammed until the oxide trapped charge anneals. The most careful study of annealing of bit errors appears to be by Bagatin *et al*. [BAGA10]. In most cases, only about 10% or the errors annealed with a week, but the annealed fraction was much higher in a few cases, all of which involved one 90 nm Single Level Cell (SLC) NAND flash. Micro-dose effects are something one should be aware of when analyzing heavy ion test results, even if they are not always the dominant effect.

l. Milli-Beam™ Testing

There is a relatively new system developed by Micro-RDC, Inc. that allows heavy ion testing with a collimated beam, thus providing the option of precise spatial control of the beam [CAST11]. The system uses metal plates to collimate the beam, defining, for example, a slit that exposes a stripe across the die. Two slits can define a rectangle, where the dimensions can be varied independently.

This system has only been used in one test of a nonvolatile memory [OLDH11]. In [OLDH11], the purpose was to identify regions where heavy ions caused high current events as reported in [IROM01]. The die is not visible, so some effort is required to map the chip surface, and define coordinates. The system software navigated the aperture across the die with precise control. In [OLDH11], small portions of the peripheral control circuits were irradiated one by one until all the control circuits were exposed. Fig. 8 shows a microphotograph of the die, with the light spots indicating the locations where SEFIs occurred [OLDH11]. The advantage of the system is that it can identify sensitive regions, which is not possible from a broad beam heavy ion test. The other way to identify sensitive regions of a complex die is with a pulsed laser test.

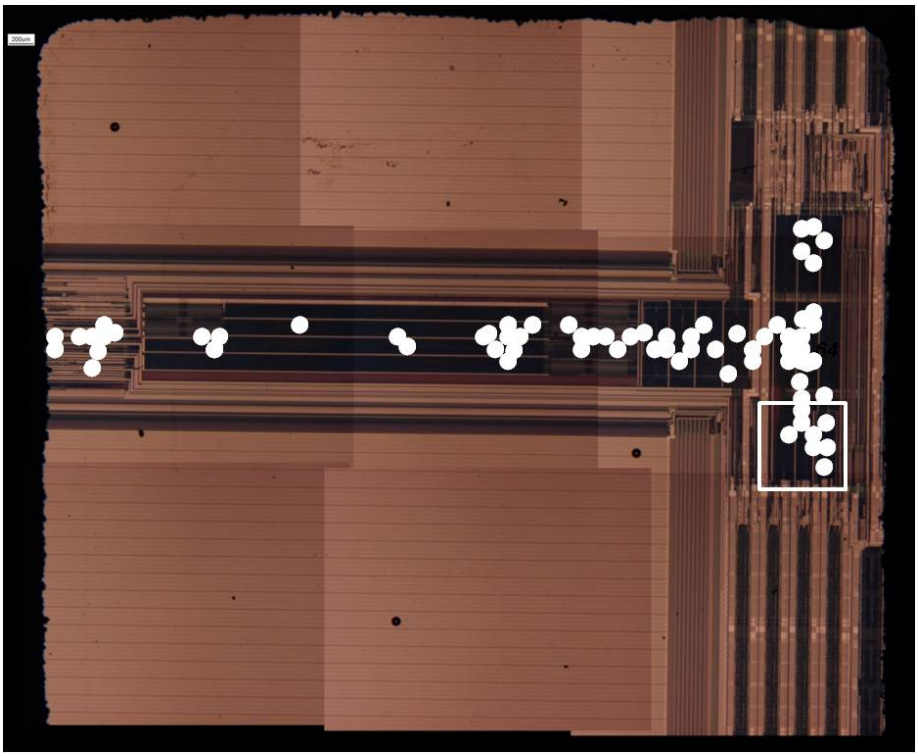

Fig. 8. Results from a Milli-Beam™test on a Micron 4 Gb NAND flash device. Light spots indicate locations where SEFIs were recorded. (After[OLDH11]).

VIII. Laser Testing

Laser testing is a technique which can be used effectively to complement heavy ion testing. Broad beam heavy ion irradiation is commonly used to identify error mechanisms and error rates, but it does not offer spatial resolution. The pulsed-laser can be focused to a spot size on scale with some transistor elements. Therefore, pulsed-laser testing can identify the sensitive regions in a memory cell or in the peripheral control logic. Another important advantage of laser testing is that it does not require an accelerator, nor does it consume scarce beam time. We will use the NRL facility as an example, to illustrate the benefits of laser testing, and also to identify issues that may arise in laser testing.

NRL actually has two laser systems. The Single Photon Absorption (SPA) system uses a 590 nm (green) light source for front-side illumination [PELL10]. This wavelength corresponds to an energy of 2.11 eV, which is above the Si band gap. So the light is strongly absorbed once it reaches the Si. In a complex commercial NVM, there is typically a lot of metal above the Si, which tends to reflect the light, so one is often unsure of the amount of light that actually reaches the Si surface, or how much is actually being absorbed. Therefore, there is considerable uncertainty in attempts to correlate incident power with effective LET in the substrate. Even so, enough light frequently gets absorbed by the substrate, leading to charge diffusion similar to that from a heavy ion hit. Identifying the sensitive locations can provide clues to single event mechanisms in complex circuits.

Oldham *et al*. have used SPA pulsed-laser irradiation to examine high current events in flash memories [OLDH12-A]. The experimental results qualitatively correlated with broad beam and Milli-Beam™ test results. The pulsed-laser test identified the sensitive locations in the peripheral control circuits that caused the SEFIs previously observed during broad beam testing. Furthermore, the

locations of the sensitive regions coincided with Milli-Beam™ test results with reasonable accuracy. Fig. 8 shows a microphotograph of the die, with the red and white spots indicating the locations of SEFIs with and without high current events, respectively [OLDH12-A]. The second NRL system is a Two Photon Absorption (TPA) system [LADB04], which uses infrared light with energy below the Si band-gap. It takes the simultaneous absorption of two photons to produce ionization in Si. Therefore, the laser has to be focused to a very small, high-intensity spot. The TPA system is normally used for back-side illumination, which may require thinning the device substrate, but it avoids problems caused by metal electrodes on the front surface. The system has an infrared viewer, which allows the experimenter to correlate the beam position with visible features on the front side of the die.

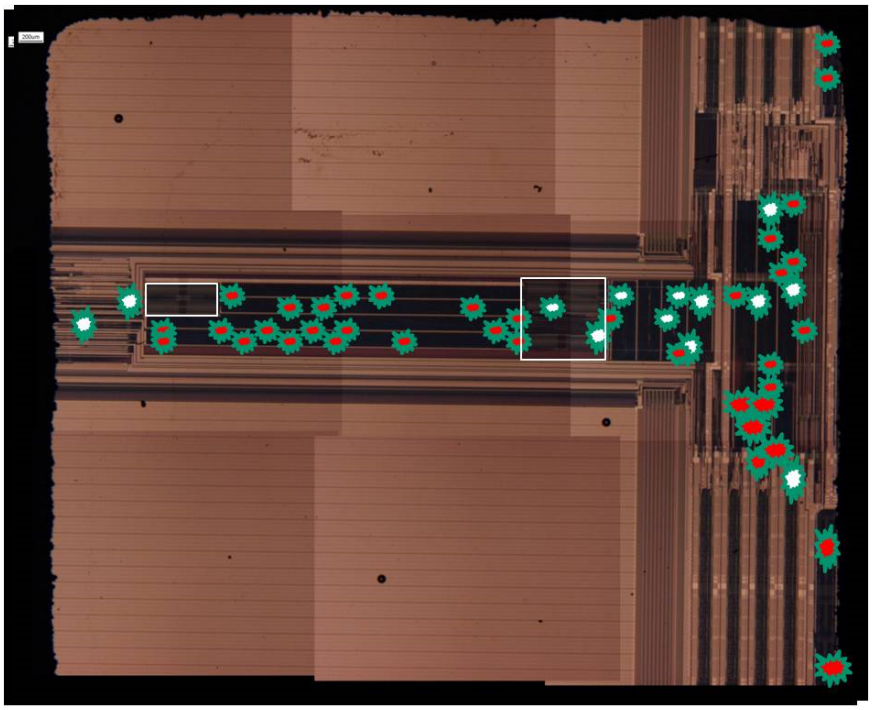

Fig. 9. Results from a laser test at NRL on a 4 Gb Micron NAND flash. The spots show the locations of 50 SEFIs. The red spots indicate SEFIs with high current events, while white spots indicate SEFIs without high current. (After[OLDH12-A]).

IX. Proton Testing

a. Background

The underlying mechanisms responsible for most proton-induced SEEs are different from the mechanisms for heavy ion-induced SEEs. Heavy ions cause SEEs by direct ionization. Proton-induced SEEs generally occur as a result of direct ionization of secondary particles produced from the initial nuclear collisions. Because nuclear interactions are involved, testing for proton-induced SEEs involves measuring the cross-section as a function of proton energy and not as a function of LET as is normally done for heavy ions. We will not discuss direct ionization by protons in detail here, except to note that it is by far the dominant charge generation mechanism in the sense that most of the energy goes into this energy loss mode. Direct ionization by protons is similar to direct ionization for other ions, except that the LET is smaller (usually significantly smaller). Because the LET is small, however, protons do not produce many of the direct ionization effects observed with other, heavier ions. Proton direct ionization

contributes primarily to TID effects, rather than SEE. However, products of nuclear interactions are observed to contribute to SEE. Protons can interact both elastically and inelastically with the semiconductor nuclei. Two useful reviews of proton interactions and rate calculations are given in [PETE97], [PETE96].

b. Whether to Test

A part can be sensitive to proton-induced SEE if the threshold LET from heavy ion testing is less than 15 MeV·cm^2/mg. The LET of 15 MeV·cm^2/mg corresponds to the LET of the secondary ions from proton-Si reactions [ONEI98].

We note that advanced unhardened commercial flash memories have threshold LETs well below 15 MeV·cm^2/mg. However, the expected proton SEE sensitivity has not always been observed for reasons that are unclear. Therefore, proton testing is recommended as a precaution. Other kinds of NVM may have higher thresholds for upset of individual cells, especially if they do not depend on storing charge. However, the control logic is likely to be sensitive to SEFIs, at low LETs, in all cases. If a part is suspected of being sensitive to SEL, it should be tested with protons. Proton-induced SEL was first observed in 1992 [NICH92], [ADAM92].

c. Beam Parameters

A careful selection of proton beam parameters is required to obtain valid data for predicting SEE rates in space. These include proton energy, flux, and fluence.

The selection of proton energy depends on what one wants to know about proton-induced SEEs. If the goal is to screen parts for single-event latchup, the highest available energy should be chosen and measurements need only be done at that energy. Ideally, the proton energy will be ≥ 200 MeV for destructive SEE tests. If the goal is to be able to predict SEU rates in space, it is necessary to measure the SEU cross-section as a function of proton energy, from threshold to saturation. The number of different energies needed depends on available beam time, cost, and the accelerator's maximum energy. The highest available energy should be used to determine the saturation cross section. An accurate prediction of SEU rates in space depends on how well the data can be fit with one of the standard functions describing the dependence of cross-section on proton energy. These will be discussed in detail later. Measurements to determine the threshold are complicated by the fact that the cross-section is small and large proton fluences are required for good statistics. Large proton fluences can cause TID damage that will destroy the part well before measurements with good statistics are obtained. In this case, it is advisable first to do measurements at high proton energies and then at lower proton energies.

The proton flux should be selected based on two factors: 1) the time required to reach a specified fluence and 2) the expected error rate. Because of the significant cost involved for beam time, all fluxes should be chosen with an eye toward saving beam time. However, too high a proton flux could lead to the system being overwhelmed and not operating properly. In the case of SEL, inaccurate values of fluence could occur due to the time lag between when an event occurs and when the beam is switched off. Good practice suggests that results from an initial run could help determine an appropriate flux for subsequent runs.

The fluence used for a test is determined by error statistics. If the number of single events is N, then the error in the measurement is given by $N^{0.5}$. For an error equal to 10%, $N^{0.5}/N$ must be equal to 1/10, which sets N = 100. To satisfy this criterion, at least a hundred SEEs must be logged. (For a detailed discussion of statistical error, refer to an introductory book on statistics.) This is sometimes not possible near the SEE threshold, where the cross-section is small and the device might be damaged as a result of proton-induced TID or DD before the required number of SEE have been logged. (Although frequently

ignored, plots of SEE cross-section versus energy should include error bars.) If there are no events, then the maximum fluence to test to is determined by the mission requirements. If the requirements are not known, testing should stop either after a fluence of 10^{11} protons/cm^2 or after destruction of the part, whichever comes first.

d. Packaging

Because high-energy protons will penetrate the covers of most devices without losing much energy, devices can be tested without having to remove the lid or plastic covering the part. For example, a 100 MeV proton has a penetration depth in aluminum of 3.7 cm. At low energies the protons have a much smaller range. For example, the range of 20 MeV protons in an alloy such as iconel is less than 1 mm and the lid or plastic should be removed. The best approach is to use the SRIM radiation transport tool [SRIM] to calculate the range of protons with low energies in materials. If the energy loss is significant, it is advisable to remove the packaging if possible, or get an accurate measure of the thickness and use SRIM to calculate the energy loss.

e. Beam Control

At UCD, control of the beam is passed on to the test engineer. To gain familiarity with the software controlling the beam, one should try a few "dry runs" with no parts exposed. Also, to avoid accumulating fluence when the DUT is not operating, the DUT should be turned on and operating properly before being exposed to the proton beam. For the same reason, the beam should be turned off before the DUT is characterized at the completion of the test.

f. Testing at Speed

Electronic devices must be tested at the same speed as that used in space because the error rate cross-section has been shown to be frequency-dependent, i.e., the higher the speed, the greater is the error rate. If the part is operated at a speed lower than intended, an underestimation of the error rate will result. Therefore, the bandwidth of the test setup should be commensurate with the test speed needs and this precludes having the test equipment outside the vault. The test equipment must be placed in the vault and controlled via Ethernet or other system that allows remote control. Leading edge flash memories currently operate at 40 MHz, which is easier to accommodate than the GHz frequencies of some other technologies, especially with FPGA-based test systems, such as the NASA LCDT (Low Cost Digital Tester) [HOWA06]. Other kinds of nonvolatile memories may differ somewhat in operating frequency, but they do not generally operate at extremely high frequencies either.

g. Sample size

The number of DUTs of the same kind that can be tested will depend on many factors, including their size (which determines how many can be tested at once), beam time available, budget and number of devices available. Occasionally, one may have to settle for testing a single device because of cost or availability of parts, but with commercially available NVMs, this is not usually the case. The DOD Test Guideline document recommends at least three parts for SEE testing, and five parts for TID testing. Since a proton test can be focused on either TID or SEE, either number might apply. COTS devices, known to have a large variability in radiation response, certainly require testing of at least a few parts.

h. MBUs

Multiple Bit Upsets (MBUs) are a common problem in volatile memories exposed to heavy ions. They have also been reported in NVMs, especially floating gate flash, for heavy ion exposure [CELL07]. So far, they have not been reported in NVMs from proton irradiation, but it is possible they will be,

because secondary ions produced by proton interactions can duplicate the angular incidence reported in [CELL07]. But, as with primary heavy ions, the affected cells have to lie within the ion track, which will tend to reduce the rate at which MBUs will occur. Charge sharing in the Si substrate, which is the dominant mechanism in volatile memories, will not play a role.

i. Data Analysis

Proper data analysis is an important aspect of proton-induced SEE testing. Proton testing is required for predicting SEE errors rates in space and involves the measurement of the proton-induced SEE cross-section as a function of energy. Two different theoretical approaches have been used to calculate the energy dependence. The first approach is to perform a Monte Carlo calculation (such as CUPID [FARR82]), which will not be discussed in detail here. The second is a semi-empirical approach based on the energetics of nuclear interactions. There are three different equations that one can use for fitting the data - the Bendel 1-parameter equation [BEND83], the Bendel 2-parameter equation [SHIM89] and the Weibull equation [WEIB51]. The Bendel 1-parameter equation is less accurate than the others, and is no longer widely used, particularly if data are available at more than one proton energy. More recently, the Weibull equation and the error function have been used to fit the data. They have more adjustable parameters and so require more data points.

Most SEE cross-section curves resulting from proton testing are saturated at proton energies above 100 MeV. This involves a single measurement at an energy greater than 100 MeV. In contrast, it generally requires more than one measurement to determine the threshold. For confirmation that the measurements agree with the theory, cross-sections could be measured at additional energies, but the actual number of energy values depends on budget and accelerator availability. Another approach to determine whether the proton cross-section is reasonable is to use Petersen's Figure of Merit (FOM) [PETE83], [PETE98], [NORM04].

J. TID Concerns (Micro-Dose)

We will discuss TID testing in detail in the next section. Here we limit the discussion to TID issues unique to proton testing. It is rarely cost effective to use protons for TID testing, due to the higher cost of accelerator time relative to a ^{60}Co cell or a 10 keV X-ray source. Some issues that can arise in proton testing are relatively unimportant for nonvolatile memories. Proton testing can cause displacement damage, but, displacement damage is generally not an important effect in digital CMOS circuits, including NVMs, because they are majority carrier devices. Similarly, NVMs are all CMOS, and not bipolar technology, so lengthy ELDRS (Enhanced Low Dose Rate Sensitivity) testing is not an issue. Both X-rays and gamma rays are high-energy photons that produce radiation damage via ionization of the atoms making up the oxide. Even though photons are very different from protons, the concept of absorbed dose to describe energy loss applies to both and depends on LET. In fact, data suggests that there is very little difference between a rad(SiO_2) generated by protons or by photons in the energy range of the most widely used proton sources. In general, there is little difference in the charge generation process for different kinds of radiation sources, but there can be a difference in the amount of charge which recombines, and therefore, in the amount of charge which escapes recombination. For high-energy protons, greater than about 10 MeV, the yield of charge is approximately at the geminate recombination limit [MCLE89], [OLDH03], [PEAS01], which is what would be expected in a ^{60}Co irradiation. The most commonly used proton sources – UC Davis, IUCF, and TRIUMF – all have energies well above 10 MeV, which means that there should not be issues related to recombination. We will discuss other total dose mechanisms issues in more detail in the next section, which deals with TID testing.

There is one puzzling TID-related result from proton testing of flash memory that deserves to be mentioned, however. In a proton test, apparent TID failures were observed at doses significantly lower

than failure levels from ^{60}Co testing of the same part [69]. There was also wide variation in the failure level from part to part in the proton test. The authors speculated that the result could be due to micro-dose effects, where a single secondary particle in the right place could deposit enough dose to disable a critical transistor. A mechanism that depends on only a single particle was attractive, because it could explain the apparent randomness of the failures. However, there was no direct evidence to confirm this speculation. Other proton tests by the same authors have not produced similar results. Even so, others conducting proton tests of flash memories might want to be aware of the result.

X. TID (Gamma) Testing

The fundamental ionizing dose mechanisms in MOS technology have been studied extensively for many years, and, although additional details emerge every year, a reasonable degree of understanding has been achieved. This understanding has been captured in numerous reviews [MCLE89], [OLDH08], [WINO89], [OLDH89], [SCHR04], [OLDH99]. We will not discuss these mechanisms in great detail here.

a. Sources and dosimetry

TID testing is usually done with either a ^{60}Co source or a 10 keV X-ray source, manufactured by Aracor Corp. The ARACOR system uses a silicon PIN diode to determine the dose to the silicon chip, which it does very accurately. However, TID failures are usually due to effects in the oxide layers on top of the silicon substrate, and there are two main differences in dosimetry between the Si substrate and the oxide layers: the first is recombination [OLDH03] and the second is dose enhancement, which arises because CPE (charged particle equilibrium) is not maintained [OLDH03].

For ^{60}Co exposures, testing is usually done in accordance with MIL-STD-883, Test Method 1019 [DOD10]. Condition A is used for high dose rate testing of CMOS components, which is the normal test condition for NVMs. Usually, the facility has a calibration, traceable to NIST (National Institute of Standards and Technology), of the activity of the source when new. This calibration, combined with the half-life of ^{60}Co (approximately five years), allows the activity of the source to be calculated very accurately for any later date. However, even when the activity of the source is known, there are practical complications to be reckoned with. For example, it has been shown that low energy photons can scatter off the walls of the test cell, significantly changing the photon spectrum seen by the target material [KERR85]. Practically speaking, the actual spectrum is different at nearly every ^{60}Co source. For this reason, TM-1019 prescribes the use of a Pb/Al filter. The idea is that the lead foil absorbs the secondary photons, and the Al layer inside the lead is thick enough to stop all the secondary electrons produced by photon interactions in the lead. Even so, it is usually necessary to do active dosimetry, and actually measure the dose to the sample. At the GSFC ^{60}Co source, describe above, air ionization gauges are mounted inside the Pb/Al box next to the samples to read out the actual dose. Another popular method at other gamma ray sources is to use thermoluminescent dosimeters (TLDs) [KERR89]. TLDs are popular because they are small, inexpensive, and passive, meaning they require no instrumentation during exposures. They also retain accurate information for years, and are useful over a wide range of doses (10^{-2} to almost 10^{6} rad). There are several materials which can be used for TLDs, but the two most common ones are LiF and CaF_2:Mn (manganese doped calcium fluoride).

b. Bit errors and annealing

Total ionizing dose causes shifts in the threshold voltage distribution of flash memory cells [CELL04-B]. A cell with logic 0 has an excess of electrons in the floating gate. So the cells with logic 0 have a positive threshold voltage. TID shifts the threshold voltage distribution in the negative direction. Conversely, TID shifts the threshold voltage distribution of the logic 1 cells in the positive direction.

Cellere *et al*. found that a total dose in excess of 100 krad(Si) was needed to induce errors in the memory cell arrays for flash devices featuring 8.3 nm tunnel oxide [CELL04-B], so the memory arrays are fairly TID hardened, without additional hardening by design techniques. The TID-induced failures typically originate from control logic circuits, as we discuss further below.

Flash memories have demanding retention specifications, meaning that they have to retain information for long periods without being refreshed. For single level cell flash memory (SLC, storing one bit per cell) ten year retention is a typical reliability specification. The stored charge may only be represented by a few dozen electrons. Therefore the oxide leakage currents, which are too small to measure directly, can still cause reliability failures. As a result, tunnel oxide thicknesses have remained at or near 10 nm, even though horizontal scaling has continued at a rapid pace. Consequently, the structures of flash memory cells are looking more and more like skyscrapers. The oxides in the individual cells are, therefore, much thicker than the oxides in some parts of the peripheral control logic. The TID response of unhardened commercial flash memories can vary widely, but some of them can tolerate 100 krad(SiO_2) or even more [OLDH06-A]. If a high enough dose is delivered to the tunnel oxide, positive charge can build up in the oxide to the point that it offsets the negative charge on the floating gate, and cells programmed as zeroes (floating gate full of electrons) will be read as ones (floating gate empty of electrons). When this happens, the cell can be reset by erasing and rewriting, after which it still works properly, if the Erase and Write circuits still work properly. Both the Erase and Write operations require injecting large numbers of electrons through the tunnel oxide, which tends to neutralize positive charge in the tunnel oxide. This, in turn, tends to restore the proper charge balance to the cell. We have already mentioned that TID-induced bit errors can also anneal spontaneously [SCHM07], [GUER06].

c. Functional (destructive) failures

We have already discussed the charge pumps in connection with destructive events in heavy ion testing [DICK76], [TANZ97]. Functional failures in TID testing are very similar, in that typically, either the Erase function is lost, or the Write (Program) function is lost, or, frequently, both are lost at the same time. The charge pumps put out high voltages (20 V) compared to the normal 3.3 V power supply. Here, the point is that circuit elements that have to accommodate these higher voltages have thicker oxides, which may make them more sensitive to radiation damage. As in heavy ion testing, the functions that fail in TID testing are always functions that require the charge pumps, which is why the failures are normally attributed to the charge pumps. As we have discussed in connection with heavy ion testing, [IROM01] showed that functional failures are correlated with a significant drop in charge pump output voltage. [OLDHAM11-B] and [CHEN] have observed similar results in TID testing of advanced commercial flash devices. In most cases, the functional failures are characterized by the inability to perform the block erase operation.

d. Non-flash NVMs

For nonvolatile memories other than flash, the nonvolatile storage element is often very resistant to radiation damage. For example, magnetic memories and phase change memories have been tested [OBRY10], [COCH10], [OLDH06-A], [NGUY01], [BENE91] and the individual cells have been shown to be very resistant to radiation. However, if the peripheral control logic is unhardened commercial CMOS, it will have the limitations typical of unhardened commercial CMOS of the the same technology node.

e. NAND vs. NOR differences

Up to this point, the discussion of flash memories has focused on NAND flash, because it is the leading commercial technology, with a much larger market compared to the NOR flash technology. Also, NAND flash has higher bit density than NOR flash. NAND flash scales more aggressively than NOR

flash. In addition, there is a significant difference in TID radiation response. NOR flash typically fails at much lower TID levels than NAND flash [RADH]. The most likely reason for this difference lies in the different architectures. NAND flash has a serial organization, which is illustrated in Fig. 2. In the NAND organization, the bit cells are in a string, which typically has 32 cells in a 4 Gb or 8 Gb part. There is only one set of Source line contacts for the entire string. On the other hand, for the NOR organization, each cell has its own complete set of contacts. The reason NAND has a better TID response appears to be that radiation-induced leakage current from a given bit cell is blocked by the other cells in the string, since most of the cells are off, most of the time. There is nothing to block the leakage current from a cell in the NOR architecture. Therefore, NOR memories are inherently more sensitive to radiation-induced leakage current.

XI. Combined Effects (Reliability Effects after Radiation Exposure)

The microelectronics in space systems will gradually accumulate ionizing dose throughout the mission lifetime. So, an important question has been raised – can radiation exposure affect the long term reliability of nonvolatile memories and flash memories in particular? The conclusion from the limited test data available is that the reliability of flash memories appears to be relatively good after radiation exposure, although reliability degradation has been reported under limited conditions. The results depended on the dose level as well as the method used to accelerate the aging process. There are two methods for accelerated aging, both of which are standard techniques in the industry. The first method involves a high temperature bake (100 °C) at overstress bias conditions (110% of V_{dd}). Results from using this method produced a clear, statistically significant difference in the retention failure rate between the irradiated samples and unirradiated controls. Fig. 10 shows the results from an investigation by Oldham *et al*. for Samsung 8 Gb flash devices that are initially irradiated, then bias stressed at 100 ^{o}C [OLDH12-B]. The results showed that retention errors increase with accumulated dose. Furthermore, the retention errors showed a nonlinear dependence on dose, where the error count increased by approximately 20× from a 4× increase in dose (50 to 200 krad(Si)). Micron 16 Gb flash devices showed qualitatively similar behavior for retention errors on total dose. This test method was used to simulate the case of a memory storing critical program codes, which are intended to be rewritten rarely, if ever.

The second aging method involves repetitive Program/Erase (P/E) cycles, which simulates the aging of mass storage memories, which are rewritten with reasonable frequency. Results obtained by this method produced no statistically significant difference between irradiated samples and unirradiated controls, although the irradiated samples had slightly more errors than the controls in all cases. In these tests, the parts were exposed to 50 krad(SiO_2), because at higher doses other radiation-induced degradation mechanisms will dominate, leading to functional failure. Oldham *et al*. [OLDH11-B] concluded that these parts may have showed statistically significant retention failure rates at higher doses. Endurance test results on Micron 8 Gb devices also showed no statistically significant difference between the irradiated and unirradiated samples [OLDH09-A].

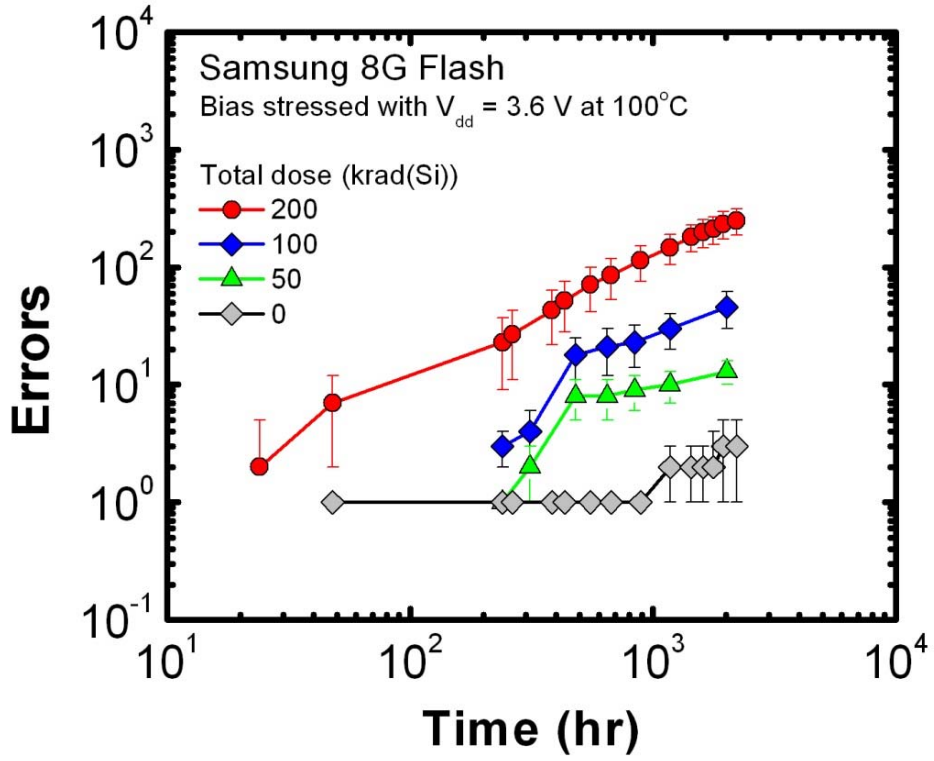

Fig. 10. Retention error vs. time for Samsung 8G Flash devices irradiated to different total dose levels (plus an unirradiated control), and bias stressed with V_{dd} = 3.6 V at 100°C. The retention errors increase with increasing total dose. (After[OLDH12-B]).

Bagatin *et al*. [BAGA11] used a different test method than either of those in [OLDH11-B]. They monitored the change in the threshold voltage (ΔV_T) of floating gate transistors, which are fabricated as test structures. The samples were irradiated to 30 krad(SiO_2) and aged by baking. They concluded that the ΔV_T was small enough that the parts would not have suffered retention failures in less than the ten year retention period that manufacturers typically cite. This conclusion is somewhat different from the results reported in [OLDH11-B]. However, the dose levels and the test samples are different. Both groups agree that the dose could make a difference in the retention rates. It is also true that the failure rate in [OLDH11-B] was on the order of one bit cell out of every 10^8. In [BAGA11], there were zero failures out of a much smaller number of test structures. We will discuss error correction in the next section, but here we note simply that the observed error rates are low enough that standard error correction schemes would be expected to correct all the errors without difficulty.

The results present a complicated picture. TID exposure has a significant effect on retention/reliability in some cases, but not in others. Critical variables include how the parts are intended to be used, and the expected mission lifetime dose (which means the orbit and duration). We have not discussed it in detail here, but there are also significant differences among manufacturers, as one might expect. There may be cases where it would be wise to include retention testing after TID exposure as part of the qualification process for nonvolatile memories. This decision will depend on the dose and on how the parts will be used, and such testing will not always be necessary. In some cases, though, it should be considered.

In heavy ion testing, there is no question that retention failures can, and do, occur [OLDH05]. The cumulative V_T distribution for Programmed cells (that is, stored zeroes), develops a tail of low V_T cells, which have been damaged by the heavy ions. When the part is rewritten, the initial V_T distribution is recovered, approximately. However when the part is allowed to sit undisturbed, a tail of damaged bits with low V_T builds up within a few days to several weeks, because residual damage to the oxide allows charge to leak off the floating gate, again. Essentially identical results were also presented by Cellere *et al*. at the same conference [CELL05]. Oldham *et al*. provided an explanation of the underlying physical mechanism [OLDH11-A]. The ionization density of high LET ions can be significant enough such that coulomb repulsive forces between adjacent atoms break the chemical bonds, forcing the atoms to move apart [FLEI75]. This process can disrupt the insulating structure, leading to increased leakage current. Below the threshold LET, the coulomb forces are not strong enough to disrupt the lattice before other processes neutralize the ionization.

XII. Error Correction

Although we have not used error correction in any of our tests up to now, it is our plan to use error correction in future tests. The retention test results in [OLDH11-B] illustrate the reasons for doing this. No error correction was used in the tests described in [OLDH11-B]. However, the manufacturer's specifications assume that error correction will be used. It is likely that most of the errors reported in [OLDH11-B] would be corrected by a robust error correction scheme. For example, in an 8 Gb part, the pages are 4Kx8 for data storage, with 128 extra addresses (128x8, or 1024 bits) for error correction. Using a simple Hamming code [SROU06], a packet of 2^N bits requires N+1 check bits for single error correction (SEC). Single Error Correction/Double Error Detection (SEC/DED) requires one more check bit, or N+2 bits. The space set aside for error correction is then sufficient to correct one bit in each 512 bit packet: 512 bits is 2^9, which requires 10 bits for SEC or 11 bits for SEC/DED. Each page contains 64 packets of 512 bits, so 640 or 704 of the 1024 bits will be used. Since there are 64 pages/block, each block can have up to 4K bits corrected (64 bits per page x 64 pages). Since the entire memory contains 4K blocks, the entire memory can have up to 16M bits corrected. This analysis assumes the errors are distributed so that no two fall in the same 512 bit packet, which is far from a random distribution. A few hundred randomly distributed errors are extremely unlikely to result in two errors falling in the same packet. For a memory with N packets, there is an approximate formula for the number of errors necessary before the probability of a double (that is, uncorrectable) error reaches 50% [MCEL85]. The formula is $(N\pi/2)^{1/2}$. For example, in the 8 Gb memory discussed above, with 16M 512 bit packets, there would be about a 50% chance of one double error after about 5000 single errors. Thus, the apparent retention "failures" that we are reporting probably would not be real system-level errors. It is our view that error correction should be included in future tests, since it plays a critical role. We also note that some in the industry believe error correction techniques will have to more robust in the near future because of continued scaling. That is, as the number of electrons distinguishing a one from a zero decreases, errors will become more common, and, therefore, harder to deal with. Therefore, it will be increasingly important to test the application-specific error correction scheme properly.

XIII. Displacement Damage

Normally, nonvolatile memories are not tested for displacement damage effects because CMOS processes are not sensitive to displacement damage. Displacement damage affects primarily minority carrier lifetime, and CMOS transistors are majority carrier devices. For this reason, nonvolatile memories are very resistant to neutrons, such that neutron testing can be omitted. However,

displacement damage can also occur during proton or heavy ion testing, which are typically performed to evaluate SEE susceptibility. As we have already discussed, protons and heavy ions can undergo a nuclear reaction, producing secondary particles with LETs higher than that of the primary particles. Most of the energy from these secondary particles will be deposited as ionization, which is the reason we usually address ionization issues first. However, there is a possibility that a displacement damage cluster can be generated at the end of the ion track [LIND63], [SROU06], [PALK08], [SROU88]. Srour and Palko examined the nature of these clusters, and concluded that the incident particle produces a primary knock-on atom (PKA), which may, depending on its energy, produce a cascade of secondary knock-on atoms. At the end of their range, these atoms have a high LET, and can melt a small region of the Si target material. This melted Si is quenched before it can re-crystallize, leaving an amorphous inclusion, which is typically on the order of 5 nm in diameter. However, these displacement damage clusters appear to have little effect on CMOS nonvolatile memories thus far. On the other hand, damage clusters could have more effect if feature sizes reach and exceed 5 nm.

XIV. Conclusion

We have reviewed the space environment and available facilities for ground testing in this guideline document. We have reviewed dosimetry techniques, both for counting particles at accelerators, and for TID testing. We pointed out five important lessons learned in reviewing heavy ion test techniques. First – angular effects are important in evaluating the radiation response of advanced NVM devices. Studies have shown important differences in the SEE response between normal and high angle incident ion strikes. Some cases even exhibit different characteristics between tilt and roll orientations at the same angle. Particles in the space environment can pass through the spacecraft at any angle. Second – one must consider the various test modes available in advanced state-of-the-art nonvolatile memories. Time and budget limitations do not allow for evaluating every test mode for every irradiation condition; therefore, one should always choose the test modes which are appropriate for the particular application. The typical test set for flash memories may include static mode (with and without bias), dynamic Read mode, dynamic Read/Write, and Read/Erase/Write. Third – the peripheral control circuits are susceptible to the most critical failure modes in flash memory devices. Radiation-induced degradation of the control circuits can result in the loss of the Erase and/or Write function. Destructive functional failures correlate with degradation of the high-voltage charge pumps, which are utilized during Erase and Write functions. Although the duty cycle for these operations will be relatively low in typical applications, the Erase and Write operating modes must be emphasized due to the severity of the functional failures. Fourth – choosing appropriate beam parameters is pertinent to a successful and representative test. Generally, one wants to keep the flux as low as possible to avoid collective effects from multiple ion hits. At the same time, one must also irradiate to a reasonably high fluence for statistical confidence. Testing to a high fluence at low flux is inefficient. Therefore one must make the necessary trade-offs among beam parameters to get the most important test results. Fifth – one must perform the appropriate analysis from ground test data to estimate the performance in flight. Tools such as CREME96 can estimate the error rate from ground test data in a given user-defined environment. The confidence level of the calculated error rate will largely depend on the quality of the test data. We also raised the question of whether the current standard test requirement (fluence of 1×10^7 particles/cm^2) is sufficient for the feature sizes in advanced submicron processes.

In addition to TID and SEE test methodologies, we have also reviewed proton testing. Generally, direct ionization of protons contributes to TID damage but not SEE in flash or other NVM devices. (In other kinds of volatile memories, there is a minimal contribution from very low energy protons, but this has not been observed in nonvolatile memory testing, probably because the threshold LET for SEE effects is higher.) Single-event effects are primarily due to secondary ions, resulting from nuclear

interactions. The effects of proton-induced SEE are limited in flash memory. We have reviewed TID testing issues, including micro-dose effects. Micro-dose can contribute to retention failures in flash memory. We have also discussed synergistic effects – reliability degradation resulting from radiation exposure. Radiation exposure can worsen the retention characteristics of flash memory. These synergistic reliability effects may need to be considered in qualification testing in some cases. We have also reviewed displacement damage, which does not appear to be a significant factor in nonvolatile memory testing.

Furthermore, we have discussed the implementation of error correction for radiation testing. Error correction software will be able to correct most of the single-bit and double-bit errors. Therefore we expect that these error types will not become a realistic concern for actual applications. On the other hand, error correction schemes cannot handle the large scale errors or functional failures that can originate from the control logic. Radiation-induced degradation in the control circuits remains the most critical concern for radiation hardness assurance of flash memory. The significance of cell array errors and control circuit errors may evolve in the future. Some manufacturers have indicated that more complex error correction will be necessary in the near future to counteract the effects of continued scaling. Our view is that error correction should be a part of any radiation test, since the error correction scheme is a critical component of nonvolatile memory technology.

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